UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,872	03/12/2004	Andy L. Lee	ALTRP193/ A1047	8348

51501 7590 06/19/2006

BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
CRAWFORD, JASON	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,872	LEE ET AL.	
	Examiner	Art Unit	
	Jason Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,13,16-20,26 and 27* is/are rejected.

7)☒ Claim(s) *9-12,14,15 and 21-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/12/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments

Applicant's amendments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

The indicated allowability of claims 18-26 is withdrawn in view of the newly discovered reference(s) within Cliff (US 5689195). Rejections based on the newly cited reference(s) follow.

Miscellaneous

The Applicant has canceled claim 3, therefore only Claims 1, 2 and 4-27 are to be examined in this Office Action.

Drawings

The drawings are objected to because in Figs 7-14 and 18, the reference number 700 does not point directly to the redundancy circuit; and in Figs 7-14 and 18, it is not clear whether the reference number 700 points to the dashed lines or the multiplexer. However it is noted that the dashed lines already identified by 104 and the multiplexer by 702. Corrected drawing sheets in compliance with 37 CFR 1 .121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." if a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 and 2 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 3 and 4 of copending Application No. 10/801,242. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claim limitations found within this application regarding claims 1 and 2 can be found and are anticipated within claims 3 and 4 of the copending application, including but not limited to a carry chain, a first and second path, a multiplexer, a first and second series of logic elements.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 7-8, 13, 16-20 and 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Cliff (US 5689195).

In regards to Claim 1, Cliff discloses of a carry chain in a logic array block of Fig 11 having a set of logic elements (20a-f in Fig 11), the carry chain comprising a first path (through 20a) connecting a first series of logic elements (30s in 20a, each element

20a-f contains a series of logic elements 30, see Fig 1) in the logic array block, wherein the logic elements in the first series (30 in 20a) is a subset of the set of logic elements in the logic array block (30 is a subset of each 20), a second path (through 20b) connected a second series of logic elements (30s in 20b) in the logic array block, wherein one or more of the logic elements in the second series are not in the first series (the 30s located within 20a are NOT the same ones within 20b) and a multiplexer (750b) having a first and second input (one corresponding from the output of 20a and the other corresponding to the output from 20b), wherein when the first input is selected, a carry signal (54) is propagated through the first series (30s in 20a) of logic elements and wherein when the second input is selected, the carry signal (54) is propagated though the second series (30s in 20b) of logic elements. (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

In regards to Claim 2, Cliff discloses of the logic elements of the first series (30s in 20a) are a subset of the logic elements of the second series (30s in 20b). (each 30 is a set within a set of identical elements 30, therefore rendering them subsets, Fig 1, 11)

In regards to Claim 5, Cliff discloses of the carry chain of Fig 11 further comprising a multiplexer (750d) located at a bottom portion of the logic array block. (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

In regards to Claim 7, Cliff discloses of a first multiplexer (750a) configured to bypass a first portion of the carry chain (20a) wherein the logic elements in the first series (30s in 20a) are located within the first portion (20a) and a second multiplexer (750b) configured to bypass a second portion of the carry chain (20b) wherein the logic

elements in the second series (30s in 20b) are located in the second portion (20b). (in Fig 11, if the correct inputs are selected, the portions are bypassed, Column 20 Lines 54-67 and Column 21 Lines 1-20)

In regards to Claim 8, Cliff discloses of the first multiplexer (750a) includes a first input (of 54 coming into the figure) connected to a beginning of the first series (30s in 20a), a second input connected to an end of the first series (output from 20a), an output (from 750a) connected to a beginning of the second series (30s in 20b) and wherein the second multiplexer (750b) includes a first input (from the output of 20a) connected to the end of the first series (30s in 20a), a second input connected to an end of the second series (30s in 20b). (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

In regards to Claim 13, Cliff discloses of a first carry chain (of elements 30 within 20a, see Fig 1, 11) defined by the first path (through 20a), at least a second carry chain (of elements 30 within 20a, see Fig 1, 11) defined by the second path (through 20b) wherein each of the logic elements in the second series are not in the first series (the 30s located within 20a are NOT the same ones within 20b). (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

In regards to Claims 16 and 17, Cliff discloses of digital system comprising a programmable logic device (Fig 1) including the carry chain of Claim 1 (in Fig 11). (Column 4 Lines 10-33 teaches that carry chains connect one module (or programmable logic device) to another, which corresponds to a system)

In regards to Claim 18, Cliff discloses of a programmable logic device in Fig 1 comprising an array of logic elements grouped into a plurality of logic array blocks (20) and a carry circuit (in Fig 11) disposed within the logic array block, the carry circuit configured to operate in a first mode and a second mode (corresponding to which input of the two are selected of 750b) wherein when the carry circuit operates in the first mode (first input, corresponding to the output of 20a, is selected), a carry signal (54) is propagated through a first series (30s in 20a, see Fig 1) of logic elements within the logic array block and wherein when the carry circuit (750b) operates in the second mode (second input, corresponding to the output of 20b, is selected) a carry signal (54) is propagated through a second series (30s in 20b, see Fig 1) of logic elements within the logic array bock, the first series (30s in 20a) being a subset of the second series (30s in 20b) of logic elements (each 30 is a set within a set of identical elements 30, therefore rendering them subsets).(Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

In regards to Claim 19, Cliff discloses of a multiplexer (750b) having a first and second input (one corresponding from the output of 20a and the other corresponding to the output from 20b), wherein when the first input is selected, a carry signal (54) is propagated through the first series (30s in 20a) of logic elements and wherein when the second input is selected, the carry signal (54) is propagated though the second series (30s in 20b) of logic elements. (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

In regards to Claim 20, Cliff discloses of a first multiplexer (750a) configured to bypass a first portion of the carry chain (20a) wherein the logic elements in the first series (30s in 20a) are located within the first portion (20a) and a second multiplexer (750b) configured to bypass a second portion of the carry chain (20b) wherein the logic elements in the second series (30s in 20b) are located in the second portion (20b). (in Fig 11, if the correct inputs are selected, the portions are bypassed, Column 20 Lines 54-67 and Column 21 Lines 1-20)

In regards to Claim 26, Cliff discloses of digital system comprising a programmable logic device (Fig 1) including the carry chain of Claim 1 (in Fig 11). (Column 4 Lines 10-33 teaches that carry chains connect one module (or programmable logic device) to another, which corresponds to a system)

In regards to Claim 27, Cliff discloses of method of forming a carry chain in a logic array block of Fig 11 having a set of logic elements (20a-f in Fig 11), the method comprising forming a first path (through 20a) connecting a first series of logic elements (30s in 20a, each element 20a-f contains a series of logic elements 30, see Fig 1) in the logic array block, wherein the logic elements in the first series (30 in 20a) is a subset of the set of logic elements in the logic array block (30 is a subset of each 20), forming a second path (through 20b) connected a second series of logic elements (30s in 20b) in the logic array block, wherein one or more of the logic elements in the second series are not in the first series (the 30s located within 20a are NOT the same ones within 20b) and a multiplexer (750b) having a first and second input (one corresponding from the output of 20a and the other corresponding to the output from 20b), wherein when the

first input is selected, a carry signal (54) is propagated through the first series (30s in 20a) of logic elements and wherein when the second input is selected, the carry signal (54) is propagated though the second series (30s in 20b) of logic elements. (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff (US 5689195).

In regards to Claim 4, Cliff discloses of a carry chain in a logic array block of Fig 11 having a set of logic elements (20a-f in Fig 11), the carry chain comprising a first path (through 20a) connecting a first series of logic elements (30s in 20a, each element 20a-f contains a series of logic elements 30, see Fig 1) in the logic array block, wherein the logic elements in the first series (30 in 20a) is a subset of the set of logic elements in the logic array block (30 is a subset of each 20), a second path (through 20b) connected a second series of logic elements (30s in 20b) in the logic array block, wherein one or more of the logic elements in the second series are not in the first series (the 30s located within 20a are NOT the same ones within 20b) and a multiplexer (750b) having a first and second input (one corresponding from the output of 20a and the other

corresponding to the output from 20b), wherein when the first input is selected, a carry signal (54) is propagated through the first series (30s in 20a) of logic elements and wherein when the second input is selected, the carry signal (54) is propagated though the second series (30s in 20b) of logic elements. (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

Cliff does not directly disclose of the multiplexer being positioned at the middle portion of the logic array block.

The positioning of the multiplexer is simply a particular design choice and is not patentably distinct over the circuit taught by Cliff (See *In re Japikse, MPEP 2144.06)*

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to change the positioning of the multiplexer taught by Cliff to be able to fabricate the carry chain in a way that has easier access to the carry input.

In regards to Claim 6, the Cliff discloses of a multiplexer (750d in Fig 11) having a first and second input (one corresponding from the output of 20c and the other corresponding to the output from 20d), wherein when the first input is selected, a carry signal (54) is propagated through a first series (30s in 20c) of logic elements of a preceding logic array block and wherein when the second input is selected, the carry signal (54) is propagated though a second series (30s in 20d) of logic elements of a preceding logic array block. (Fig 1, 11, Column 5 Lines 33-36, Column 20 Lines 54-67 and Column 12 Lines 1-20)

Cliff does not directly disclose of the multiplexer being positioned at the top portion of the logic array block.

The positioning of the multiplexer is simply a particular design choice and is not patentably distinct over the circuit taught by Cliff (See *In re Japikse, MPEP 2144.06)*

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to change the positioning of the multiplexer taught by Cliff to be able to fabricate the carry chain in a way that has easier access to the carry input.

Allowable Subject Matter

Claims 9-12, 14-15 and 21-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Crawford whose telephone number is 571-272-6004. The examiner can normally be reached on Monday - Friday 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rex Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMC

Rexford Barnie

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER